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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,639	09/18/2003	Hiroki Koga	N34771600WD1	6100

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,639	KOGA, HIROKI	
	Examiner	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,17-23 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,17-23 and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/991093.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 9-16 are canceled in the amendment filed on 18 Sept. 2003.

Claim Objections

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

There is no claim 24.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 5-7, 21, 23, 25 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6573132 to Uehara et al.

Regarding claim 1, Uehara discloses a semiconductor device in fig. 1 including an insulated gate field effect transistor (IGFET), comprising: a gate electrode 21, column 6 line 65,

of the IGFET having a lower layer electrode 21a, column 7 line, formed on a gate insulating film 13, column 6 line 64, and an upper layer electrode 21b, column 7 line 2, formed on the lower layer electrode 21a; a cap film 31, column 6 line 65, formed on the upper layer electrode 21b, a first nitride film 32, column 6 line 67, on a side surface of the upper layer electrode 21b; an oxide film 13 (upper portion of layer 13) on a side surface of the lower layer electrode 21a; and an etching stopper film including a second nitride film 33, column 6 line 67, formed on the outside of the first nitride film 31 and oxide film 13.

Regarding claims 2-3, 6-7, 23, 25 the process limitations "thermal nitride film" in claim 2, "rapidly heated thermal nitride' in claim 3, "thermal oxide film' in claims 6, 23, and "nitride film is formed with CVD' in claims 7, 25 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 5, Uehara discloses the semiconductor device further including an interlayer insulating film 38, fig. 1, formed to cover the gate electrode of the IGFET; a contact hole 39, fig. 3c, opened in the interlayer insulating film 38 to expose a source/drain region 15, fig. 3c, of the IGFET; and a conductor filling 40, column 7 line 37, the contact hole and electrically connected with the source/drain region 15.

Regarding claim 21, Uehara discloses a semiconductor device in fig. 1, comprising: a first transistor formed in a first region comprising a first upper layer gate electrode 21b formed on and in electrical connection with a corresponding first lower layer gate electrode 21a, a first insulating film 13 formed on a side surface of the first lower layer gate electrode 21a and not on the side surface of the first upper layer gate electrode 21b, fig. 1, a second insulating film 32 formed on a side surface of the first upper layer gate electrode 21b, the second insulating film 32

having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material, and a first etching stopper film 33 formed on the outside of the first and second insulating films, fig. 1.

With respect to the 'thermal growth' limitation, it does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

5. Claims 21, 26-28 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6521963 to Ota et al.

Regarding claim 21, Ota discloses a semiconductor device in fig. 25, comprising: a first transistor formed in a first region comprising a first upper layer gate electrode 51b, column 12 line 15, formed on and in electrical connection with a corresponding first lower layer gate electrode 4C, a first insulating film 14, column 20 line 38, formed on a side surface of the first lower layer gate electrode 4C and not on the side surface of the first upper layer gate electrode 51B, fig. 25, a second insulating film 25B, column 20 line 43, formed on a side surface of the first upper layer gate electrode 51B, the second insulating film 25B having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material, and a first etching stopper film 7, column 10 line 14, formed on the outside of the first and second insulating films, fig. 25.

With respect to the 'thermal growth' limitation, it does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 26, Ota discloses the semiconductor device wherein the first lower layer gate electrode 4C has a greater length that the first upper layer gate electrode 51B, fig. 25.

Regarding claim 27, Ota discloses the semiconductor device further including: a second transistor formed in a second region, fig. 4 that is applied to Fig. 25, comprising a second upper layer gate electrode 51B formed on and in electrical connection with a corresponding second lower layer gate electrode 4C, a third insulating film 14 formed on a side surface of the second lower layer gate electrode 4C and not on the side surface of the second upper layer gate electrode 52B, a fourth insulating film 25B formed on a side surface of the second upper layer gate electrode 51B, the fourth insulating film having a lower thermal growth rate with respect to the second upper layer gate electrode material than the thermal growth rate of the third insulating film with respect to the second lower layer gate electrode material, a second etching stopper film 7 formed on the outside of the third and fourth insulating films 14/25B, a first transistor source/drain region 6 extending laterally below the second etching stopper film 7, fig. 25, and a second transistor source/drain region overlapping a portion of the first transistor source region that does not extend laterally below the second etching stopper film (portion next to S/D 6).

With respect to the 'thermal growth' limitation, it does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 28, Ota discloses the semiconductor device further including a third transistor source/drain region 9 having a different concentration than either the first or second transistor source/drain regions extending laterally below the first etching stopper film, fig. 25, (LDD structure)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6573132 to Uehara.

Regarding claims 4, 22, Uehara does not disclose the semiconductor device wherein the first nitride film 32 has a film thickness of approximately 2 to 5 nm.

But, Uehara discloses the nitride layer 32 has the thickness of about 10 nm, column 8 line 30. Accordingly, it would have been obvious to one of ordinary skill in art to use thickness teaching of Uehara in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

8. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5985712 to Ooishi in view of US 6521963 to Ota et al.

Regarding claim 17, Ooishi discloses a semiconductor device in fig. 5E including a first region (left) and second region (right), comprising: a first gate electrode (left) of a first IGFET in the first region having a first lower layer electrode 11, fig. 5A, formed on a first gate insulating film 3a and a first upper layer electrode 12, fig. 5A, formed on the first lower layer electrode 11,a first cap film 13, fig. 5B, formed on the first upper layer electrode 12; a first film 7b, fig. 5B,

formed on a side surface of the first upper layer electrode 12; a first oxide film 13a on a side surface of the first lower layer electrode 11; a second gate electrode (right) of a second IGFET in the second region having a second lower layer electrode 11 formed on a second gate insulating film 3b, fig. 5A, and a second upper layer electrode 12 formed on the second lower layer electrode 11; a second cap film 13 formed on the second upper layer electrode 12; a third film 7b on a side surface of the second upper layer electrode 12, fig. 5B, a second oxide film 13b, fig. 5B, on a side surface of the second lower layer electrode 11, and wherein the first IGFET includes a lightly doped drain 5a, fig. 5B, and the second IGFET does not include a lightly doped drain, fig. 5C.

But, Ooishi does not disclose a first and third film comprises nitride and first and second etching stopper film including a fourth nitride film formed on the outside of the first and third nitride and first and second oxide films.

However, Ota reference discloses a semiconductor device comprising a nitride film 25B on the upper electrode 51B, and etching stopper film including a nitride film 7, fig. 25, formed on the outside of the first nitride 25B and oxide films 14. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to combine the nitride film on the upper electrode and etching stopper film including a nitride film formed on the outside of the first nitride and oxide films teaching of Ota with Ooihi's device, because it would have prevented the oxidation of the gate metal layer and realized lower resistivity as taught by Ota, see abstract.

Regarding claims 18-19, Ooishi discloses the semiconductor wherein the first region is a semiconductor memory device and wherein the second region is peripheral circuit region, column 6 line 18-25.

Regarding claim 20, Ooishi discloses the semiconductor device further including: a first contact 28a, fig. 5E, providing an electrical connection to a first source/drain region 8C of the first IGFET; a second contact 19, fig. 5C, providing an electrical connection to a second source/drain region 5b of the second IGFET.

But, Ooishi does not disclose a first spacing from the first contact to the first gate electrode is greater than a second spacing from the second contact to the second gate electrode. However, Ooishi discloses a general spacing between the firs and second contacts from the gate. Accordingly, it would have been obvious to one of ordinary skill in art to use teaching of Ooishi in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

9. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6521963 to Ota et al in view of US 5985712 to Ooishi.

Regarding claim 29, Ota discloses the semiconductor device further including the first transistor includes at least a third transistor source/drain region (LDD).

But, Ota does not disclose a first contact in electrical connection with the third source/drain region, and isolated from the first lower layer gate electrode by a first insulating thickness; and a second contact in electrical connection with the first and

second source/drain regions, and isolated from the second lower layer gate electrode by a second insulating thickness that is greater than the first insulating thickness. Such contact is conventional to make electrical contact to S/D region as discloses in Ooishi, fig. 5E.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
19 Aug. 2004

LONG PHAM
PRIMARY EXAMINER